

HZC6.2Z4

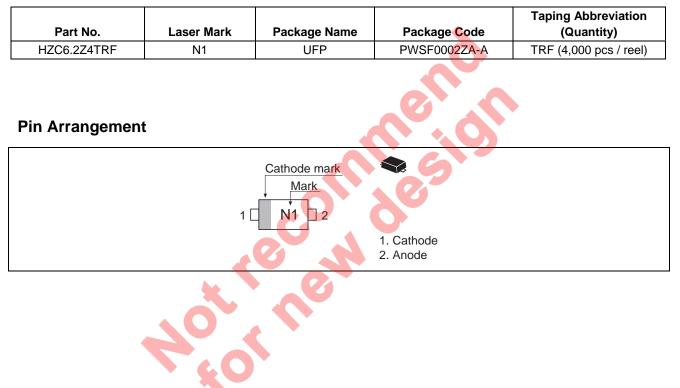
Silicon Planar Zener Diode for Surge Absorb

REJ03G1720-0100 Rev.1.00 Jan 13, 2009

Features

- Low capacitance (C = 4.0 pF max) and can protect ESD of signal line.
- Ultra small Flat lead Package (UFP) is suitable for compact and high-density surface mount design.

Ordering Information



Absolute Maximum Ratings

Symbol Item Value Unit Pd * 150 mW Power dissipation °C Junction temperature Тj 150 °C Storage temperature Tstg -55 to +150

 $(Ta = 25^{\circ}C)$

Note: See Fig.2.

Electrical Characteristics

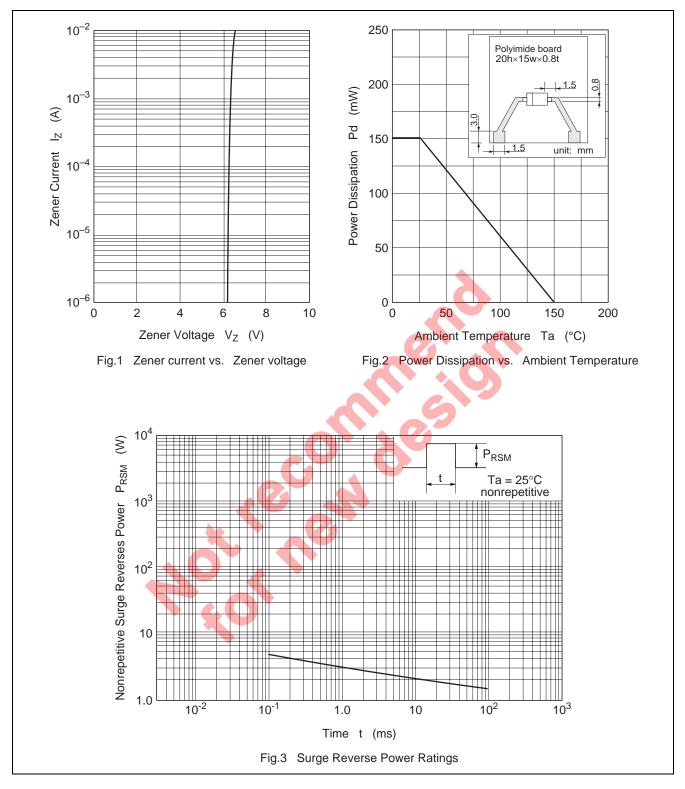
						$(Ta = 25^{\circ}C)$
Item	Symbol	Min	Тур	Max	Unit	Test Condition
Zener voltage	Vz	5.90	—	6.50	V	$I_Z = 5 \text{ mA}, 40 \text{ ms pulse}$
Reverse current	I _R	—	—	3	μA	V _R = 5.5 V
Capacitance	С	—	—	4.0	pF	$V_R = 0 V$, f = 1 MHz
Dynamic resistance	r _d	—	—	60	Ω	$I_z = 5 \text{ mA}$
ESD-Capability *1*2	—	8	—	—	kV	C = 150 pF, R = 330 Ω , Both forward
						and reverse direction 10 pulse

Notes: 1. Failure criterion ; $I_R > 3 \mu A$ at $V_R = 5.5 V$.

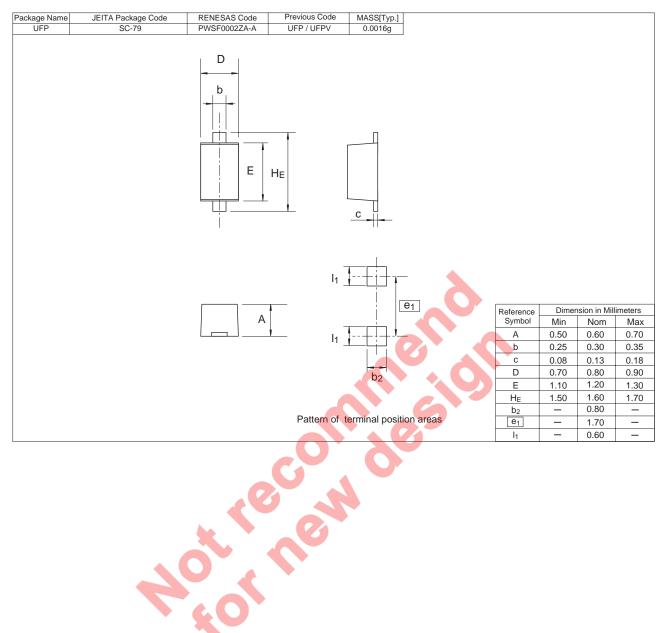
2. Between cathode and anode.

.p of the Lase test and 3. In the UFP package, some lead is exposed because the tip of the lead is used as the cutting plane. Therefore, the solderability of the lead tip has been ignored. Please test and confirm before use.

Main Characteristics



Package Dimensions



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